REMARKS

Introduction

This Reply is in response to the Office Action of December 29, 2005. Reconsideration of this application in view of the following remarks is respectfully requested.

Drawings

The informal drawings that were originally filed with the patent application were objected to by the Draftsperson. Formal drawings that comply with Patent Office requirements are accordingly submitted herewith to replace the informal drawings. Approval of the formal drawings is respectfully requested.

Claim Objections

The claims have been amended to address the informalities identified by the Examiner.

In particular, claims 1, 3, and 21 have been amended to use the "take into account" language preferred by the Examiner.

Claim 4 has been amended to address the antecedent basis issue for "the amounts of signals".

Claim 18 has been amended to address the antecedent basis issue for "the expected".

Applicant has not added the suggested comma after the word "high" in claim 19, because the additional comma would unnecessarily break the phrase "using the information on the expected fraction of the given signal's operation that the signal is to be high to produce configuration data" into two disjoint parts.

The phrase "using a logic design system to generate" has been added to claim 17, obviating the need to amend claims 18 and 20 to address the antecedent basis issue for "the logic".

The Prior Art Rejections

Claims 1, 2, 5, 7, 9, 13, and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hart et al. U.S. patent application No. 2004/0216074. Claims 3, 4, 6, 8, 10-12, and 14-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hart in view of the article entitled "Design Techniques for Gate-Leakage Reduction in CMOS Circuits" by Rafik S. Guindi et al. These rejections are respectfully traversed.

Applicant's invention relates to logic design systems for programmable logic devices.

As explained in applicant's specification, it is becoming possible to fabricate transistors and other integrated circuit components with increasingly small dimensions. Although it is generally desirable to shrink component sizes as much as

possible to reduce costs and improve performance, smaller transistor gate sizes can lead to problems such as undesirable gate leakage effects.

In accordance with applicant's invention, a programmable logic device design system is provided that addresses gate leakage problems. The logic design system uses computer-aided design tools to produce configuration data for a programmable logic device. The tools are aware of gate leakage effects, so that when the programmable logic device is programmed using the configuration data, the resources of the programmable logic device perform desired custom logic functions specified by a logic designer while reducing gate leakage. This allows power consumption due to gate leakage to be minimized while maintaining required levels of logic performance.

Applicant's independent claims are directed to various aspects of using a logic design system that takes gate leakage effects into account.

Independent claim 1 is directed to a method for using a logic design system to implement a logic design in a programmable logic device. With the method of claim 1, the logic design system generates configuration data that takes into account power consumption due to gate leakage effects.

Independent claim 7 is directed to a method for using a logic design system to minimize power consumption in a

programmable logic device. In the method of claim 7, the logic design system produces configuration data that implements a desired logic design while routing signals to reduce power consumption due to gate leakage effects.

Independent claim 14 is directed to a logic design system that uses placement and routing tools including a gate leakage optimizer tool to produce configuration data for a programmable logic device. The configuration data that is produced causes signals to be routed to transistor gates on the programmable logic device based on the likelihood of those signals to be high or low to reduce power consumption due to gate leakage.

Independent claim 17 also addresses gate leakage. In the method of claim 17, configuration data for a programmable logic device is generated that minimizes power consumption due to gate leakage in transistors in logic gate stacks. The method of claim 17 involves lowering gate leakage by producing configuration data that routes signals based their likelihood of being high.

Independent claim 21 is directed to a computer-readable medium having instructions for causing computing equipment to execute a method in which configuration data is produced that takes gate leakage effects into account to minimize gate leakage power consumption.

In the Office Action, it was suggested that independent claims 1, 7, and 21 were anticipated by the Hart reference. Applicant disagrees.

Hart describes structures and methods for selectively applying a well bias to portions of a programmable logic device. There is no description in Hart of gate leakage problems, let alone techniques for overcoming these problems. Hart is completely silent with respect to gate leakage effects.

In the Office Action, it was suggested that FIG. 7 and paragraphs 14-16, 25, 60, and 60 of Hart were pertinent to applicant's claims. However, none of these portions of Hart or any other portion of Hart even mentions gate leakage.

Paragraph 14 of Hart describes how a positive well bias can increase drain-source leakage current in an inactive transistor. Paragraph 15 describes how fixed function devices can be designed in which positive well bias is applied to speed-critical circuits to avoid positive well bias problems. Paragraph 16 describes difficulties associated with addressing positive well bias problems in the context of programmable logic devices. None of these paragraphs makes any mention of gate leakage effects.

The well bias effects described in paragraphs 14-16 of Hart are unrelated to gate leakage. In well biasing schemes, a well bias voltage is applied to the body terminal of a

transistor to change its threshold voltage. Changing the threshold voltage of a transistor changes its drain-source current when inactive. (See, e.g., paragraph 14 of Hart, in which it is explained that positive well biasing affects the amount of current flowing through an inactive transistor.) Gate leakage effects are entirely different. Gate leakage arises because the insulating material in a transistor's gate is not perfect. As a result, a quantum-mechanical effect known as "tunneling" allows current to flow across the gate into the transistor's source and drain. Gate leakage effects are strongly influenced by a transistor's gate-to-source and gate-to-drain voltages, not its well bias voltage.

The other cited portions of Hart are also inapplicable to applicant's claimed invention.

Paragraph 25 of Hart relates to negative well biasing effects that can decrease drain-source leakage. Gate leakage is not mentioned.

Paragraphs 60 and 61 of Hart relate to identifying critical paths in a circuit design. Paragraph 91 lists certain types of circuits that are said to be suitable for Hart's well biasing techniques. None of these paragraphs relate to gate leakage effects.

Hart presents a flow chart in FIG. 7. The flow chart shows how a circuit can be evaluated to determine timing delays

(step 701), to compare timing delays to determine slower and faster paths (step 702), and to generate a configuration data file enabling well biasing of transistor(s) on one or both paths (step 703). None of the steps of FIG. 7 relate to gate leakage effects.

Because claims 1, 7, and 21 are directed to logic tools that take account of gate leakage effects, whereas Hart does not even acknowledge that gate leakage effects exist, claims 1, 7, and 21 are not anticipated by Hart. Claims 2-6 depend on claim 1 and are allowable because claim 1 is allowable. Claims 8-13 depend on claim 7 and are allowable because claim 7 is allowable.

Independent claims 14 and 17 are also allowable. In rejecting claims 14 and 17, it was acknowledged that Hart does not take into account transistor stacking effects. To make up for this deficiency in Hart, the Office Action turned to Guindi.

The Guindi paper describes design techniques for reducing gate leakage in complementary metal-oxide-semiconductor circuits, but does not make up for the deficiencies in Hart. The portion of the Office Action rejecting claims 14 and 17 states that "Hart et al. teaches the configuration data generation/production to reduce power consumption due to gate leakage, including receiving the logic design ... " and goes on to propose that it would be obvious to combine Guindi with Hart

to further these goals. As explained above, however, Hart does not teach generating configuration data to reduce power consumption due to gate leakage. Hart does not even recognize that gate leakage is a problem, let alone address possible solutions to the problem.

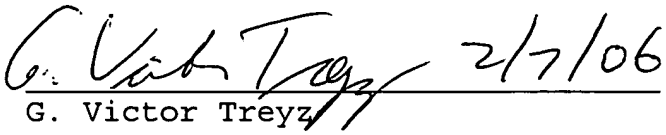
The proposed motivation for combining the Hart and Guindi references for purposes of the §103(a) rejection is therefore based on a mistaken premise. Because Hart does not disclose any techniques for taking gate leakage into effect, there is no prior art support for combining Hart and Guindi as urged in the Office Action. Claims 14 and 17 are therefore patentable. Claims 15 and 16 depend from claim 14 and are patentable because claim 14 is patentable. Claims 18-20 depend from claim 17 and are patentable because claim 17 is patentable.

Conclusion

The foregoing demonstrates that claims 1-21 are patentable. This application is therefore in condition for

allowance. Reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,



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